PHOTOMASK

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MAPPER: High Throughput Maskless Lithography

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ABSTRACT

Maskless electron beam lithography, or electron beam direct write, has been around for a long time in the semiconductor industry and was pioneered from the mid-1960s onwards. This technique has been used for mask writing applications as well as device engineering and in some cases chip manufacturing. However because of its relatively low throughput compared to optical lithography, electron beam lithography has never been the mainstream lithography technology. To extend optical lithography double patterning, as a bridging technology, and EUV lithography are currently explored. Irrespective of the technical viability of both approaches, one thing seems clear. They will be expensive.[1]

MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams. In this way optical columns can be made with a throughput of 10-20 wafers per hour. By clustering several of these columns together high throughputs can be realized in a small footprint. This enables a highly cost competitive alternative to double patterning and EUV alternatives. In 2007 MAPPER obtained its Proof of Lithography milestone by exposing in its Demonstrator 45 nm half pitch structures with 110 electron beams in parallel, where all the beams where individually switched on and off.[2]

In 2008 MAPPER has taken a next step in its development by building several tools. A new platform has been designed and built which contains a 300 mm wafer stage, a wafer handler and an electron beam column with 110 parallel electron beams. This manuscript describes the first patterning results with this 300 mm platform.

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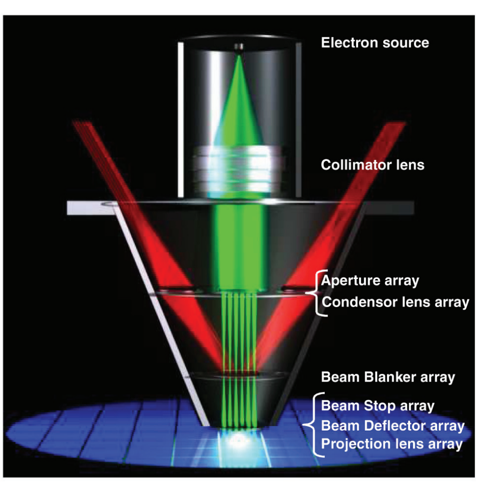

Writing time for 26 x 33 mm (incl.overhead)	2.5 sec + 2.5 sec for redundancy
Nr of beams	13,000
Gray levels	Black/white
Grid	2.25 nm
Data rate	7.5 GHz per channel
Spot size	< 25 nm
Deflection frequency	6 MHz
# of electrons per CD element	4,000
Resist sensitivity	30 μC/cm^2
Current	150 μA → 13 nA / beam
Acceleration voltage	5 kV
Stage passes per field	1
Resist	Bi / tri -layer

Figure 1. Schematic of MAPPER's massively parallel electron beam concept.

Editorial

Quo Vadis?

Bryan Kasprowicz, Photronics, Inc.

It seems that the Semiconductor Industry has been experiencing changes on a monthly basis; major logic based chip makers have not seen a viable business model and have discontinued in-house development of advanced CMOS nodes. They instead have elected to join clubs, formed partnerships or have completely outsourced these efforts to the Foundries. And more recently, after burning through their stock pile of cash, the memory industry is also going through a correction where companies are looking to partnerships, benefiting from foreign government bailouts while some even became insolvent.

This pseudo consolidation is due to a number of factors, including the economic downturn, fundamental shifts in core business strategy and market saturation / reduced demand, has had ripple effects on all of the suppliers and has left the entire industry, particularly the mask makers. Fewer customers tend to imply fewer masks.

As with any business model, the more volume, typically the cheaper the price, as you are able to amortize the cost of the investments over more parts. So with fewer buyers of advanced masks, the prices would (should) be higher in order to continue to make the necessary investments to meet the technology requirements. This is further convoluted by the timing and lack of consensus on which technology - EUV, NIL, EBDW, other – will carry us beyond 193nm immersion. This uncertainty dilutes precious resources even more. So the question of "Where are you going?" is valid. Do we as mask makers want to dabble in each of these technologies and do so independently? Does it make sense given that the refined advanced CMOS business model has the Foundries, along with the top two or three chip-makers leading the way; each of which has a captive mask facility? And if we mask makers are to make the appropriate investments – rumor is that the 32nm class inspection tools are topping $40M for the basic model – and deliver the mask technology needed, will there be enough tape outs to the merchants using these processes to justify the expense? If not, are those few companies that survive and continue to push the ITRS willing to pay realistic prices based on these factors? (If we use history as our gauge then it is doubtful, in fact they will probably request that they be [nearly] free).

With leading-edge chip makers beginning to ramp their 45-nm designs, the 32-nm node could be delayed due to the downturn, so there is a bit of time for the mask maker before the next round of investments are going to be required. Perhaps maybe now is the time to reconsider the mask maker's business model too. Instead of the respective mask companies making these investments independently, given the projected limited volume at the 32nm and below nodes, where a back of the envelope calculation pegs a 32nm mask manufacturing line at over $150M, sans building infrastructure, with another $10M or more in blank costs, why not consider one jointly owned facility that would have all the capital required to support these nodes? This strategy can mitigate the risks and reduce the overall costs by spreading this out over the collaborative parties. Think about that for a second. The three largest merchant mask makers could collectively spend over half a billion dollars on equipment for the 32/22nm nodes alone, if pursued independently. Add another 30% to that number for redundancy and you start to approach a magical number that is typically reserved for chip makers!

There may be reluctance to consider such an approach by some, but

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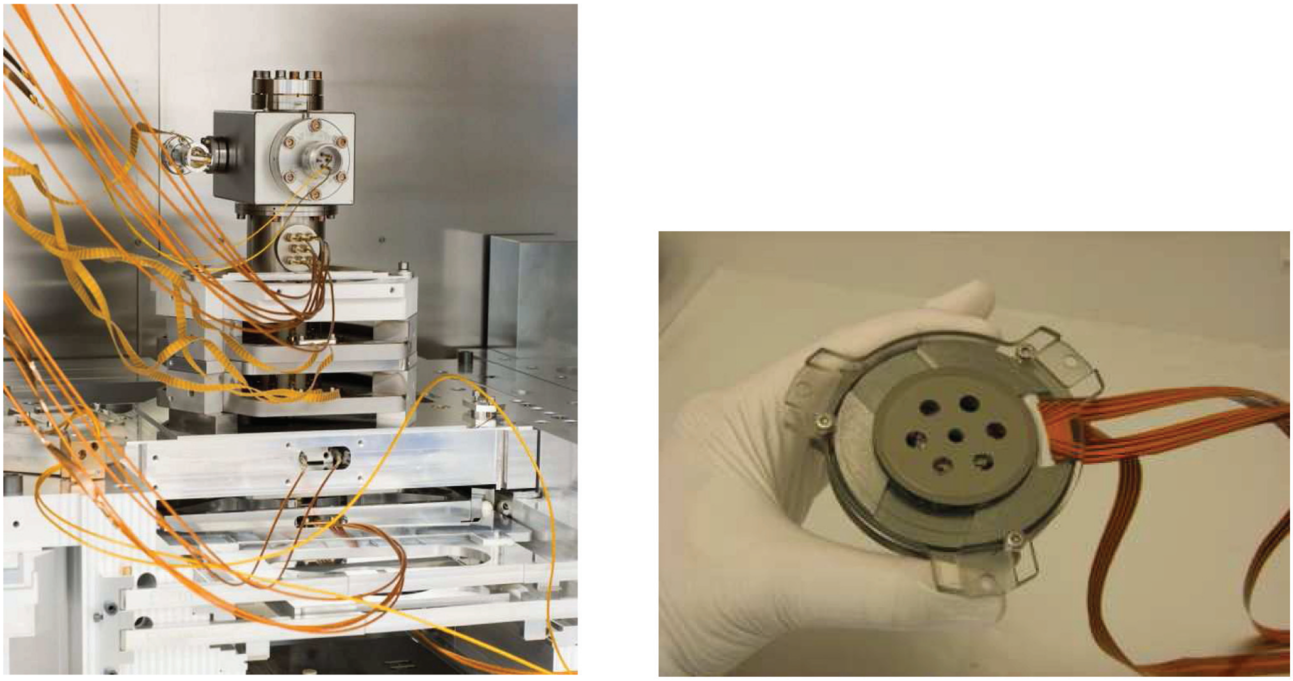

Figure 2. Overview of MAPPER's optics column (left) and an individual projection lens array (right).

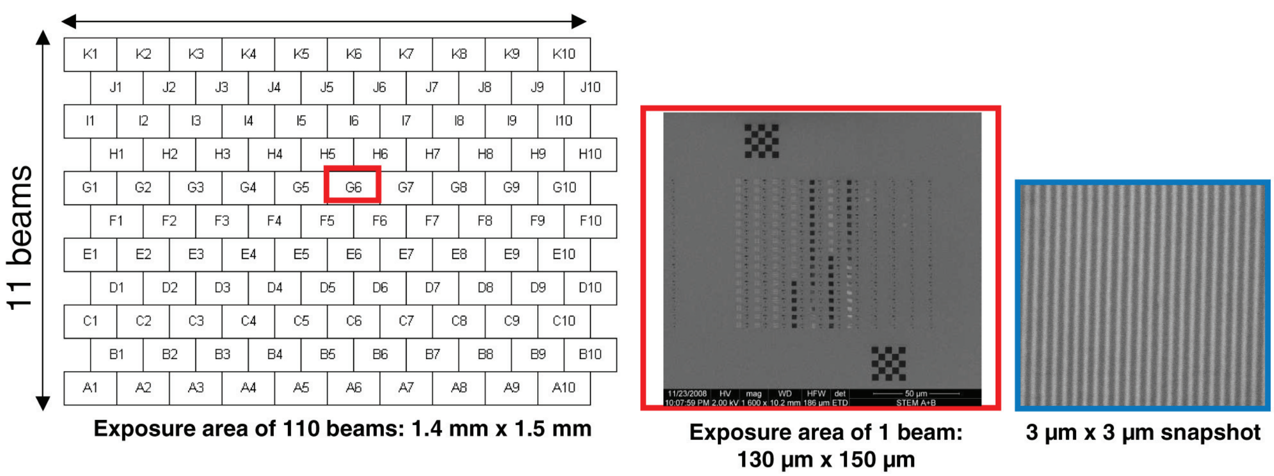

Figure 3. The arrangement of the 110 beams on the left, each exposing 130 µm x 150 µm area which is divided in 3 µm x 3 µm patterns.

1. Introduction

The MAPPER electron optics consists of a single high brightness cathode gun in space charge limit. An electrostatic collimator lens is used to create a collimated beam, see Figure 1. After the collimator the single beam is split up into 13,000 beams by the aperture array. After the aperture array the beamlets are focused by the condenser lens array in the intermediate focus plane. In this plane the beam blanker array is placed that can deflect each individual beam away from a clear aperture on the beam stop array to stop the electrons and switch off the beam at the wafer. After the beam stop array the beams are demagnified by the projection lens array and focused in the wafer plane. A deflector array is positioned between the beam stop array and the projection lens array to scan the beams over a range of 2 µm perpendicular to the wafer stage movement at a frequency of 6 MHz with a positioning accuracy of 1 nm.

In MAPPER's current machine the optics contains 110 electron beams and the targeted resolution is 45 nm half pitch, see Figure 2.

2. Explanation exposure sequence

The exposures shown in this manuscript are static exposures. An x- and an y- deflector are used to expose 110 times an area

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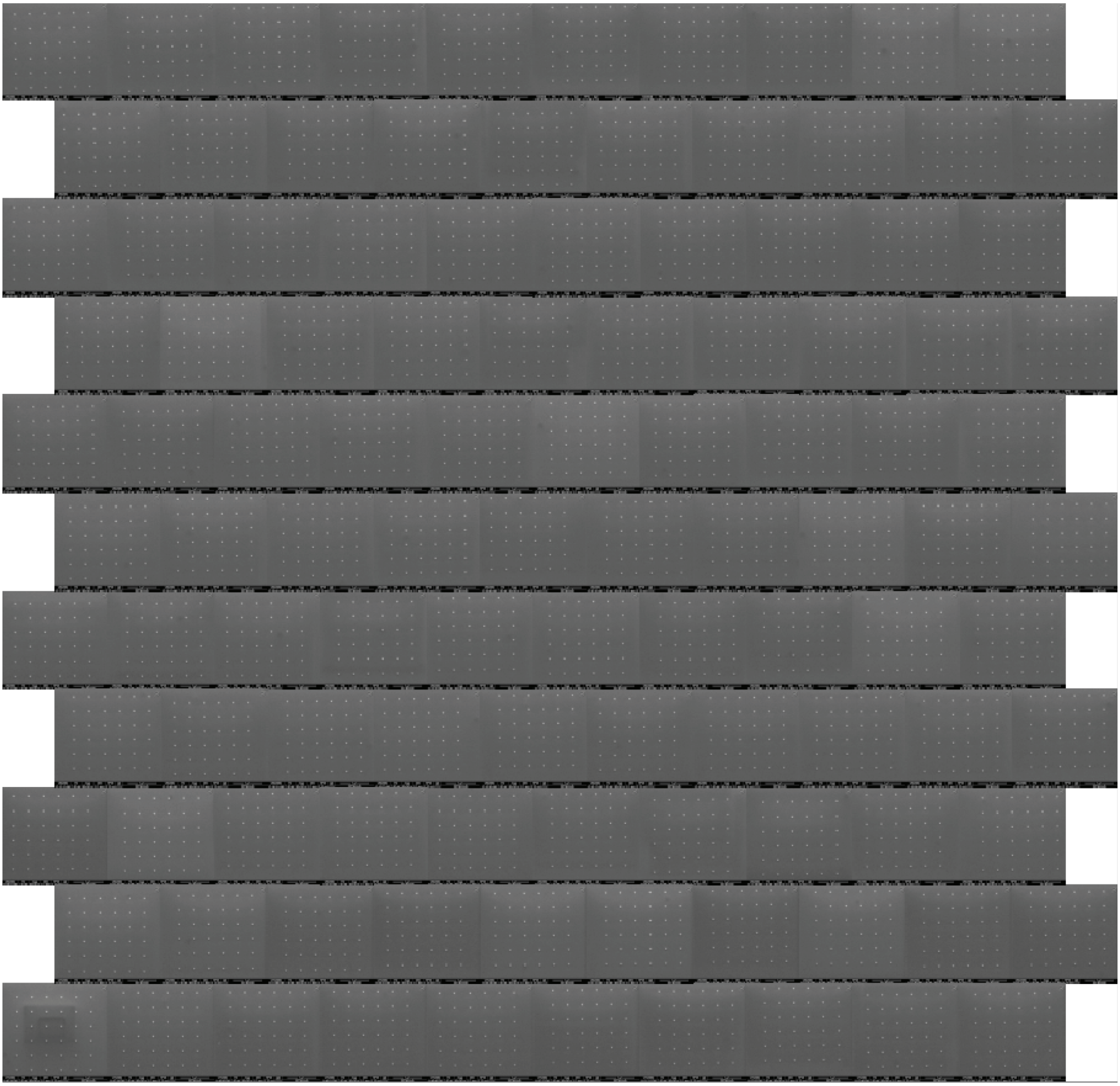

Figure 4. Overview of 110 isolated, 45 nm dot patterns exposed simultaneously.

of 3 μm x 3 μm with all the beams simultaneously. Then the wafer stage steps 5 μm to a new position and 110 new 3 μm x 3 μm areas are exposed. This is repeated 252 times resulting in 252 x 110 or 27,720 exposed patterns. Finally 110 SEM-markers are exposed. For every beam the 252 (3 μm x 3 μm) fields can contain different patterns, dose or focus settings.

The resist that is used in these exposures is 50 nm HSQ (negative) on top of a PMMA bottom layer. From Figure 4 it is clear that all beams print.

Full SEM analysis of all patterns for 110 beams is highly time consuming and therefore MAPPER has chosen for this manuscript to only inspect eleven, randomly selected beams : B2, B5, B6, B8, C2, E9, F8, G6, H2, K9 and K10.

3. Exposure results

Examples of exposures are 45 nm dense lines, both horizontal and vertical lines and 45 nm dense dots. All three exposures were exposed on the same wafer.

For analysis of CD/CDu, for each 3 μm x 3 μm area five 0.47

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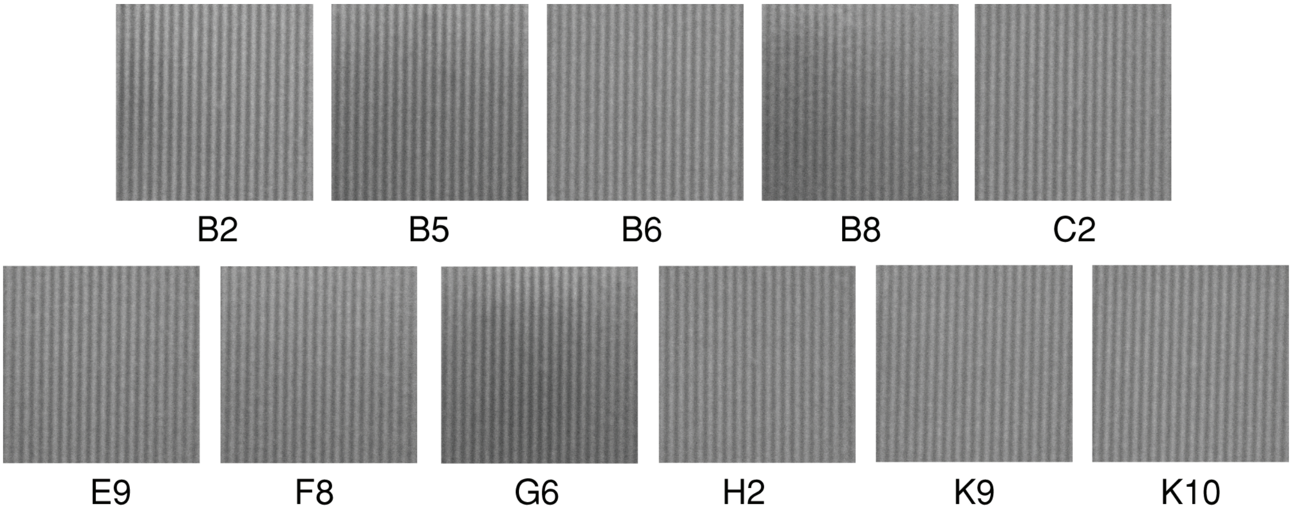

Figure 5. 45 nm dense vertical lines for the eleven selected beams.

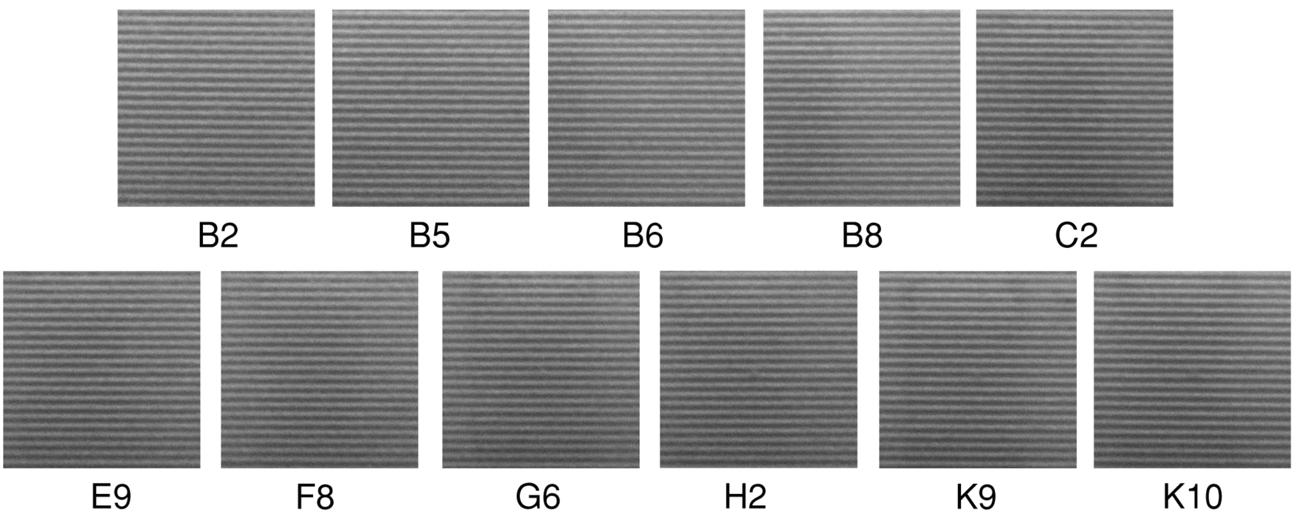

Figure 6. 45 nm dense horizontal lines for the eleven selected beams.

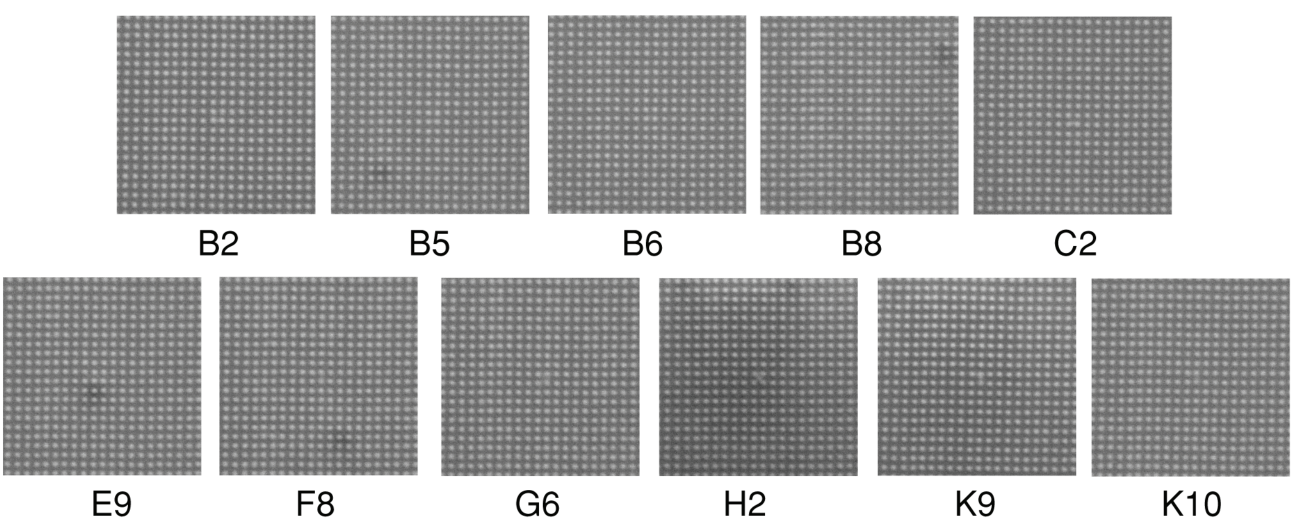

Figure 7. 45 nm dense dots for the eleven selected beams.

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Table 1. Exposure analysis results.

Pattern	CD [nm]		CD Mean -to-target [nm]	CDu [nm]
	Measured	Target	Measured	Measured
Dots dense	43.4	45.0	1.6	2.5
Horizontal dense	42.8	45.0	2.2	1.9
Verlines-dense	44.9	45.0	0.1	2.8

μm x 0.47 μm squares are drawn. Within each square, the line width is sampled at 3.6 nm intervals. The average of all line widths within a square is taken as the CD for that square. This results in the required 5 measurement points for each pattern. The average of the 5 measurement points is the CD for that pattern for that particular beam. The average over all 11 CD's for all beams is the CD for that pattern. The 3σ value of the 11 CD values is the CDu.

The result for the three patterns shown above is as shown in Table 1.

4. Conclusions

MAPPER has built its 300 mm platform based on 110 parallel electron beams in 2008. First exposures at 45 nm half pitch resolution have been performed and analyzed. On the same wafer it is observed that all beams print and based on analysis of 11 beams the CD for the different patterns is within 2.2 nm from target and the CD uniformity for the different patterns is better than 2.8 nm.

5. References

[1] B. J. Lin, presentation Sematech Lithography workshop 2008, Bolton Landing.

[2] E. Slot et al., Proc. of SPIE Vol. 6921, 69211P, (2008).

Editorial *continued from page 2.*

consider the benefits: reduced capital requirements, opportunity to take more risk with different technologies, presumably faster development due to access to advanced equipment, knowledge sharing, perhaps even licensing agreements based on the intellectual property created that is used in part to continually fund the entity. That said there are also a few logistical challenges to overcome, though none of them appear to be show stoppers aside from participation.

Many of the chip makers have already changed their model starting beginning at the 90nm node; it's time for the mask makers to morph theirs too. If chip makers are serious about their new products on these nodes they might even encourage such an arrangement so it would offer a better chance of having the enabling technology available when it is needed. And maybe it would even be affordable…

Industry Briefs

Where are the Stimulus Dollars for the Mask Makers??

The U.S. Department of Energy (DOE) has announced that the Lawrence Berkeley National Laboratory (Berkeley Lab) will receive $115.8 million from President Obama's American Recovery and Reinvestment Act.

The funds are part of $1.2 billion announced by Secretary of Energy Steven Chu on 23 March from funding allocated under the Recovery Act to DOE's Office of Science.
Funds directed to Berkeley Lab are to be used to accelerate construction of a user support building for the Advanced Light Source, one of the nation's premier research sources of x-ray and ultraviolet light, and provide additional support for research in the fields of advanced materials, energy and biology.

Funds will also be provided for other projects including a laser-based accelerator facility called "BELLA," (Berkeley Lab Laser Accelerator).

With its ability to deliver enormous energy boosts to charged particles over extremely short distances, laser-based acceleration technology could be the future of high-energy physics.

Hardmask Moving from the Fab to the Maskshop

Double-patterning generation targeted for 32-nm node and below raises many issues for photomask processing. One of the main issues is how to address the bias created post etch. Many photomask process developers have been placing focus on the resolution improvement using thin resist combined with the hardmask processing. Various hardmask materials have been shown that yield extremely high etching rates (US Patent 7365014).

Resist thicknesses have been in the area of 40-55nm; thus proving high resolution (lower aspect ratios). A recent article in The Journal of Micro/Nanolithography, MEMS and MOEMS talks about using Cr as the hardmask and reports very promising results. Specifically, the Cr-hardmask, studied in this paper, showed almost no film stress. Low to no film stress is required in order to achieve the image placement accuracy required for the double patterning.

University of British Columbia <http://www.ubc.ca>

UBC researchers put a new spin on electrons Technique could provide an easier route to 'spintronic' circuits

In the first demonstration of its kind, researchers at the University of British Columbia have controlled the spin of electrons using a ballistic technique—bouncing electrons through a microscopic channel of precisely constructed, two-dimensional layer of semiconductor.

It's the first time the intrinsic properties of a semiconductor-not external electric or magnetic fields-have been used to achieve the effect. The findings, published this week in Nature, could have implications for the development of so called 'spintronic' circuits: systems that use the directional spin of electrons to store and process data.

"The need to use high-frequency external fields to control spin is one of the major stumbling blocks in using electrons for information processing, or in a spintronic circuit," notes Joshua Folk, principal investigator on the project and Canada Research Chair in the Physics of Nanostructures. "We show that the spin of electrons can be controlled without external fields, simply by designing the right circuit geometry and letting electrons move freely through it."

The new technique uses the natural interactions of the electrons within the semiconductor micro-channel to control their spin—a technique that is a major step, but not yet flexible enough for industrial applications, notes Folk, an Assistant Professor with Physics and Astronomy who came to UBC via the Massachusetts Institute of Technology.

Electronic systems that use the spin of an electron—a quantum mechanical property that comes in two varieties: up or down—would work similarly to today's transistors, but be smaller and use less energy.

Presently, electrical charge alone is responsible for the logic functions in circuits. Power consumption by these circuits is the primary roadblock to faster, more powerful processors. A spintronic circuit has the potential to use less power by storing and manipulating a bit of information as electron spin.

Spintronic circuits may also be a viable avenue for building quantum information processing devices. The exponentially faster processing possible with such a device could have applications ranging from code breaking, to dramatically improved drug design, to simulations of complex processes in molecular systems.

Next steps by Folk and his team-working with colleagues at the Universität Regensburg in Germany-will include using new devices to gain more precise control over the alignment and trajectory of the electrons.

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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Calendar

2009

SPIE Photomask Technology

14-17 September
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
spie.org/pm

Late abstract submissions will be considered by the Chairs.

SPIE Lithography Asia - Taiwan

18-20 November
Sheraton Taipei Hotel
Taipei, Taiwan
spie.org/la

Abstracts due 2 June 2009

2010

SPIE Advanced Lithography

21-26 February
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
spie.org/al

Abstracts due 10 August 2009

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.

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